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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,217	01/27/2004	Daniel C. Guterman	SAND-01011US0	3316

28554 7590 12/13/2005

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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,217	GUTERMAN ET AL.	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 24-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,24,26-32,34 and 35* is/are rejected.

7)☒ Claim(s) *25 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/17/04, 6/17/05*, 6/27/05, 8/26/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history*.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-12 and 24-35 in the reply filed on 02 November 2005 is acknowledged.

Amendment

2. Acknowledgment is made of applicant's Amendment, filed 02 November 2005. The changes and remarks disclosed therein have been considered.

Claims 13-23 and 36-39 have been cancelled by Amendment. Therefore, claims 1-12 and 24-35 are pending in the application.

Information Disclosure Statement

3. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 17 February 2004, 17 June 2005, 27 June 2005, and 26 August 2005. The information disclosed therein has been considered.

Specification

4. Claims 5 and 34 are objected to because of the following informalities:

In claim 5, line 5, "a first non-volatile storage element" will be understood as --said first non-volatile storage element--.

In claim 34, line 5, "until said bit line reaches" will be understood as --until a voltage or a current of said bit line reaches--.

Appropriate correction is required.

Drawings

5. Figures 1-3 should be designated by a legend such as --Prior Art-- because it appears that only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-6, 8, 11, 12, 24, 26-29 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. (U.S. Pat. No. 5,969,986) in view of Holzmann et al. (U.S. Pat. No. 6,301,161).

Regarding claim 1, Wong, for example in Figs. 1, 2 and 6, discloses an apparatus for programming non-volatile storage elements (memory arrays 130 in Fig. 1), comprising: a programming circuit (including 150 generating Vpp) in communication with said non-volatile storage elements; and one or more verification selection circuits (including 150 generating Vvfy and sense amplifiers 136) in communication with said non-volatile storage elements, said one or more verification selection circuits cause a first subset of said non-volatile storage elements (for example, any one of memory arrays 130 in Fig. 1) to be subjected to first verification (associated with one of the PIPELINE write cycles in Fig. 2, corresponding to one of the memory arrays 130) concurrently while a second subset of said non-volatile storage elements (for example, another one of memory arrays 130 in Fig. 1) are subjected to second verification (associated with another one of the PIPELINE write cycles in Fig. 2, corresponding to another one of the memory arrays 130; in Fig. 2, the PIPELINE write cycles overlap in time).

Wong does not disclose that the first verification is coarse verification and the second verification is fine verification.

Holzmann, for example in Figs 3 and 5, discloses a write cycle comprising coarse verification (including steps 310-330 in Fig. 3) followed by fine verification (steps 340-360; see also Fig. 5).

Since use of coarse and fine programming/verifying in flash memories were common and well known in the art (as exemplified in Holzmann), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to implement the coarse-fine programming/verifying technique (as in Holzmann) for the write cycles of Wong, such that one PIPELINE is subjected to a coarse verification during its write cycle concurrently while another

PIPELINE is subjected to a fine verification during its write cycle (since the write cycles are staggered and overlap in time in Fig. 2 of Wong), for the purpose of providing an efficient and accurate means for programming a pipelined flash memory (see for example Holzmann, column 1, lines 38-40; see also Holzmann Fig. 2).

Regarding claims 2-4 and 12, the above Wong/Holzmann combination further discloses a set of bit lines (within the memory arrays 130 in Fig. 1 of Wong), each of said non-volatile storage elements are associated with at least one of said bit lines (inherent), said one or more verification selection circuits include one verification selection circuit for each of said bit lines (since, in Fig. 2 of Wong, the write cycle for each PIPELINE, is for one cell, with an associated bit line);

wherein: said one or more verification selection circuits include one verification selection circuit for each non-volatile storage element of a subset of non-volatile storage elements (since, in Fig. 2 of Wong, the write cycle for each PIPELINE, is for one cell, with an associated bit line);

wherein: said non-volatile storage elements are multi-state flash memory devices (see for example Wong, Fig. 6 and its brief description, and column 3, line 60 through column 4, line 12);

wherein at least one of said one or more verification selection circuits comprises: a sense circuit (130 and 140 in Fig. 1 of Holzmann, in the above combination) in communication with a first non-volatile storage element; a programming mode indication circuit (within 160 to select the coarse or fine amplitudes for programming circuit 110; see also Holzmann, column 4, lines

26-33), in communication with said sense circuit, providing an output (for example, to control 110) indicating whether said first non-volatile storage element is in a coarse programming mode or a fine programming mode based on said sense circuit (i.e., based on the result of comparator 140; see also Fig. 3); and a selection circuit (for example, within 140) in communication with said programming mode indication circuit, said selection circuit applies a coarse verification signal (for example, VIN+ΔV in step 330 in Fig. 3) to said first non-volatile storage element if said first non-volatile storage element is in said coarse programming mode and applies a fine verification signal (VIN in step 360 in Fig. 3) to said first non-volatile storage element if said first non-volatile storage element is in said fine programming mode (see Figs. 3 and 5 of Holzmann).

Regarding claim 5, the above Wong/Holzmann combination discloses an apparatus according to claim 1, wherein at least one of said one or more verification selection circuits comprises: an indicator (within 160 in Fig. 1 of Holzmann) indicating whether a first non-volatile storage element is in a coarse programming mode or a fine programming mode (to select the coarse amplitude or the fine amplitude for program circuit 110); a first switch (for example, a switch 220, 230 or 240 in Fig. 2) in communication with said first non-volatile storage element; sense circuit (including 130 and 140 in Fig. 1, for example, sensing VSF in Fig. 2) connected to said first switch and providing an output to said indicator (within 160 in Fig. 1 of Holzmann), said indicator uses said output from said sense circuit to indicate whether said first non-volatile storage element is in said coarse programming mode or said fine programming mode (to select the coarse amplitude or the fine amplitude for program circuit 110); and a second switch (within

140) in communication with said indicator (from 160; see Fig. 1) and having an output connected to said sense circuit, said second switch receiving a coarse reference signal (VIN+ΔV; see step 330 during the coarse phase in Fig. 3) and a fine reference signal (VIN; see step 360 during the fine phase in Fig. 3) and providing either said coarse reference signal or said fine reference signal at said output of said second switch in response to said indicator (i.e., the indicator in 160 determines which reference signal to compare; see Figs. 1 and 3).

The above combination does not disclose that said indicator is a storage unit storing data indicating the programming mode.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use a storage unit storing data indicating the programming mode in the apparatus of Holzmann, since use of a storage unit as a status indicator was common and well known in the art (for example, mode registers or flag registers).

Regarding claims 6 and 8, the above combination further discloses that said non-volatile storage elements are flash memory devices (see for example Wong, column 3, line 60 through column 4, line 12);

wherein: said coarse reference signal and said fine reference signal provide reference voltages (VIN and ΔV; see Figs. 1 and 3).

Regarding claim 11, the above Wong/Holzmann combination discloses an apparatus according to claim 1, and further discloses that said programming circuit includes a controller (for example, 160 in Fig. 1 of Holzmann), and said programming circuit (for example, 110 in

Fig. 1 of Holzmann) is separate from said one or more verification selection circuits (including 130 and 140).

The above combination does not disclose that said programming circuit includes a state machine.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to include a state machine in the programming circuit of the above combination to implement the process of Fig. 3 of Holzmann, since use of a state machine to implement an operating process was common and well known in the art.

Regarding claim 24, Wong, for example in Figs. 1 and 2, discloses a method for programming non-volatile storage elements (memory arrays 130 in Fig. 1), comprising: providing a programming signal (for example, Vpp in Fig. 1) to said non-volatile storage elements, said step of providing is part of a programming process that includes a first programming phase (associated with one of the PIPELINE write cycles in Fig. 2) and a second programming phase (associated with another one of the PIPELINE write cycles in Fig. 2) such that one or more of said non-volatile storage elements are in said first programming phase while one or more of said non-volatile storage elements are in said second programming phase (see Fig. 2, which shows that the PIPELINE write cycles are staggered and overlap); and performing first verification (associated with the one of the PIPELINE write cycles) for said one or more of said non-volatile storage elements that are in said first programming phase while concurrently performing second verification (associated with the another one of the PIPELINE write cycles)

for said one or more of said non-volatile storage elements that are in said second programming phase (see Fig. 2, for staggered and overlapping PIPELINE write cycles).

Wong does not disclose that the first programming phase/verification is a coarse programming phase/verification and that the second programming phase/verification is a fine programming phase/verification.

Holzmann, for example in Figs 3 and 5, discloses a programming/write cycle comprising coarse programming phase and verification (including steps 310-330 in Fig. 3) followed by fine programming phase and verification (steps 340-360; see also Fig. 5).

Since use of coarse and fine programming phases and verifications in flash memories were common and well known in the art (as exemplified in Holzmann), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to implement the coarse-fine programming phases and verifications (as in Holzmann) for the programming/write cycles of Wong, such that one PIPELINE is in a coarse programming phase and verification during its write cycle concurrently while another PIPELINE is in a fine programming phase and verification during its write cycle (since the write cycles are staggered and overlap in Fig. 2 of Wong), for the purpose of providing an efficient and accurate means for programming a pipelined flash memory (see for example Holzmann, column 1, lines 38-40).

Regarding claims 26-29 and 31, the above Wong/Holzmann combination further discloses that said non-volatile storage elements are multi-state flash memory devices (see for example Wong, Fig. 6 and its brief description, and column 3, line 60 through column 4, line 12);

using said coarse verification to determine when a particular non-volatile storage element completes said coarse programming phase (step 330 in Fig. 3 of Holzmann) and causing said particular non-volatile storage element to begin said fine programming phase (step 340 in Fig. 3 of Holzmann);

wherein: following said non-volatile storage element beginning said fine programming phase, said non-volatile storage element begins said fine verification (step 360 in Fig. 3 of Holzmann);

wherein said step of performing comprises: performing coarse verification for said particular non-volatile storage element without performing fine verification for said particular non-volatile storage element, if said particular non-volatile storage element is determined to be in said coarse programming phase (Fig. 3 of Holzmann shows that coarse and fine phases are performed sequentially and separately for a given storage element); and performing fine verification for said particular non-volatile storage element without performing coarse verification for said particular non-volatile storage element, if said particular non-volatile storage element is determined to be in said fine programming phase (similarly, Fig. 3 of Holzmann shows that coarse and fine phases are performed sequentially and separately for a given storage element).

8. Claims 7, 9, 10, 30, 32, 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. in view of Holzmann et al. as applied to claims 1, 5, 24 and 28 above, and further in view of Guterman et al. (U.S. Pat. No. 6,222,762).

Regarding claims 7, 9, 10, 30 and 32, the above Wong/Holzmann combination discloses an apparatus and a method according to claims 1, 5, 24 and 28, with the exception of said coarse reference signal and said fine reference signal providing reference currents; said coarse reference signal and said fine reference signal providing an indication of discharge times; said coarse verification and said fine verification being performed using a discharge method; causing said particular non-volatile storage element to begin said fine programming phase includes raising a bit line voltage; or said coarse verification and said fine verification are based on a bit line discharge process.

Guterman, for example in Figs. 1-3, discloses a reference signal providing a reference current (306 in Fig. 3, as an alternative to a reference voltage in Fig. 2); a reference signal providing an indication of discharge times (indicated by TSENSE in Fig. 1b); a verification being performed using a discharge method (see Figs. 1a and 1b); causing a particular non-volatile storage element to begin a programming phase including raising a bit line voltage (see Figs. 1a and 1b, in which the voltage on the bit line 101 is raised or pre-charged); and a verification are based on a bit line discharge process (see Figs. 1a and 1b).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use the bit line discharge means of Guterman, as an alternative equivalent means for a flash memory verifying operation, adapted for the coarse-fine techniques of Holzmann, such that discharge related measurements will be compared with a coarse reference value during a coarse phase and with a fine reference value during a fine phase (similar to those of Holzmann), for the purpose of providing reading/verifying means that is flexible,

consistent, adaptable and capable of covering a wide dynamic range (see for example, Guterman, column 1, lines 55-58).

Regarding claim 34, the above Wong/Holzmann combination discloses a method according to claim 24, with the exception of said step of performing comprising: pre-charging a first bit line for a first non-volatile storage element; applying a verify signal to a control gate for said first non-volatile storage element; determining a time for said bit line to discharge until said bit line reaches a predetermined value; comparing a coarse compare value to said time, if said first non-volatile storage element is in said coarse programming phase; and comparing a fine compare value to said time, if said first non-volatile storage element is in said fine programming phase.

Guterman, for example in Figs. 1-3, discloses pre-charging a first bit line for a first non-volatile storage element (see Figs. 1a and 1b, in which the bit line 101 is pre-charged); applying a verify signal to a control gate (via the word line 103) for said first non-volatile storage element (to initiate a discharge; see Fig. 1b and column 4, lines 31-48); determining a time for said bit line to discharge until a voltage or a current of said bit line reaches a predetermined value (VREF in Fig. 1b).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use the bit line discharge means of Guterman, as an alternative equivalent means for a flash memory verifying operation, adapted for the coarse-fine techniques of Holzmann, such that discharge related measurements would be compared with a coarse reference value during a coarse phase and with a fine reference value during a fine phase (similar

to those of Holzmann), for the purpose of providing reading/verifying means that is flexible, consistent, adaptable and capable of covering a wide dynamic range (see for example, Guterman, column 1, lines 55-58).

Regarding claims 35, the above Wong/Holzmann/Guterman combination further discloses that said predetermined value is a first value if said first non-volatile storage element is in said coarse programming phase (i.e., in the above combination, with Guterman's verifying means adapted for the coarse-fine verification, as in Holzmann, the reference voltage/current would have a coarse value during the coarse phase); and said predetermined value is a second value if said first non-volatile storage element is in said fine programming phase (i.e., in the above combination, with Guterman's verifying means adapted for the coarse-fine verification, as in Holzmann, the reference voltage/current would have a fine value during the fine phase).

Allowable Subject Matter

9. Claims 25 and 33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 25, the prior arts of record do not disclose or suggest a method as recited in claim 25, and particularly, providing said programming signal to a word line common to at least a subset of said one or more of said non-volatile storage elements that are in said coarse

programming phase and said one or more of said non-volatile storage elements that are in said fine programming phase.

Regarding claim 33, the prior arts of record do not disclose or suggest a method as recited in claim 33, and particularly, pre-charging a first bit line based on a coarse pre-charge signal if a first non-volatile storage element is in said coarse programming phase; pre-charging said first bit line based on a fine pre-charge signal if said first non-volatile storage element is in said fine programming phase; applying a verify signal to a control gate for said first non-volatile storage element; and allowing said bit line to discharge for a fixed period of time.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

12/12/05

Jung (John) Hur
Patent Examiner
Art Unit 2824

jhh